Benefit of ArF immersion lithography in 55 nm logic device manufacturing

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ABSTRACT

In this paper we demonstrate the many benefits of using immersion lithography that go beyond depth of focus (DOF) improvement by comparing several key features of dry and immersion lithography. Immersion lithography improves critical dimension uniformity (CDU) as well as avoiding the necessity for strong resolution enhancement techniques (RET) as compared with dry lithography. Thus it is possible to significantly reduce the burden of optical proximity correction (OPC) work with immersion lithography. With respect to imaging, we studied the sensitivity of the lithographic performances to aberrations and light source spectral bandwidth E95 fluctuations to highlight the benefits of immersion lithography. The significant improvements that have been seen in the last year in overlay accuracy, defect control and focus & leveling accuracy have been considered to be challenges to the realization of immersion lithography in mass production. Now these challenges have been met for the manufacturing requirements of 55 nm logic devices. The achievements of immersion lithography include overlay accuracy within 10 nm on resist-to-resist wafers and within 20 nm on production wafers, fewer than 10 defects per wafer, and errors of less than 40 nm in focus & leveling on full wafers. We have established a top-coat resist process. In conclusion, immersion lithography is the most promising manufacturing solution for 55 nm node logic devices, providing advantages in CDU control, and equivalent overlay performance and focus & leveling accuracy to dry ArF, without an increased level of defects. NEC Electronics has completed development and preproduction of the 55 nm logic device “UX7LS” using immersion lithography and has established the lithography technology for mass production of the UX7LS this year.

Keywords: Immersion lithography, 55nm logic device, Imaging, Overlay, CD uniformity

1. INTRODUCTION

ArF immersion lithography is the technology that will follow dry ArF, leading to smaller devices in the future, at the 65 nm node and below.13 This technology is ready for mass production, as immersion exposure tools with a numerical aperture (NA) larger than 1.0 have started to be shipped. Many technological challenges had to be overcome to bring about immersion lithography for mass production, but those challenges have been met.

In this paper, we discuss the current status of immersion lithography, focusing on the pros and cons of its introduction to a mass production environment, especially for lower NA (NA<1.0) applications by comparative factor analysis of several lithographic performance errors.

The key challenges in ArF immersion are defectivity and overlay control. There are several concerns in the immersion process such as tool contamination and/or defects due to leaching from the resist material, pattern defects, and resist profile degradation due to water droplets. Thus immersion hood improvements and a hydrophobic topcoat have been introduced. Also, overlay accuracy degradation due to water evaporation is a concern as it can cause wafer temperature instability during exposure. We have confirmed that overlay performance is well controlled by having a wafer table temperature control system in the exposure tool.

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With respect to imaging performance, DOF improvement with immersion lithography is well known. Recently the burden of OPC work for ASIC devices has become a more serious issue. Reduction in the burden of OPC work is a significant benefit of immersion lithography, as the use of strong RETS can be avoided due to improved DOF.

In this paper, we will highlight the advantages of immersion lithography by contrasting it with dry lithography for 55 nm logic device patterns with respect to robustness against imaging errors, and sensitivity to aberrations and to E95 fluctuation under optimum optical conditions. Also, we will show that overlay, focus and defect control of immersion lithography meet the requirements for 55 nm logic device manufacture due to significant improvements in the past year. Finally, we will discuss the status of immersion lithography as applied to the UX7LS 55 nm logic device by NEC Electronics.

2. IMAGING PERFORMANCE COMPARISON

Optical conditions for an 80 nm line pattern were optimized for both immersion and dry lithography. Simulation was done assuming a gate layer for a 55 nm logic device. CDUs were calculated with each error factor, assuming conventional illumination with Att-PSM, annular illumination with attenuated phase shift mask (Att-PSM) and conventional illumination with alternated phase shift mask (Alt -PSM). It was assumed that the NA was smaller than 0.93. The simulation conditions are shown in Table 1, and results in Figure 1a–c.

<table>
<thead>
<tr>
<th>Item</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation mode</td>
<td>Vector mode</td>
</tr>
<tr>
<td>CD light intensity</td>
<td>threshold</td>
</tr>
<tr>
<td>NA</td>
<td>0.78~0.93, dry &amp; wet(n=1.44)</td>
</tr>
<tr>
<td>Partial coherence</td>
<td>(sigma)</td>
</tr>
<tr>
<td>0.70~0.90@Conv.+AttPSM(6%)</td>
<td>Outer sigma=0.75~0.90@2/3 Annular + AttPSM (6%)</td>
</tr>
<tr>
<td>0.3~0.45@Conv.+Alt-PSM</td>
<td></td>
</tr>
<tr>
<td>Pattern</td>
<td>80nm L&amp;S, pitch=2000nm, 240nm, 180nm</td>
</tr>
<tr>
<td>Error</td>
<td>Mask error=+/−2nm</td>
</tr>
<tr>
<td></td>
<td>Dose error=+/−1.2%</td>
</tr>
<tr>
<td></td>
<td>Focus error=+/−50nm</td>
</tr>
<tr>
<td></td>
<td>Flare=1% (fixed)</td>
</tr>
</tbody>
</table>

Figure 1a CDU Map of Conv. + Att-PSM
Figure 1b CDU Map of Annular + Alt-PSM

Figure 1c CDU Map of Conv. + Alt-PSM

Figure 2a Optimized NA and sigma setting and CDU

Figure 2a shows a summary of CDUs for each optimum NA and sigma setting. It was found that immersion lithography gave better CDU than dry when the same exposure method was used. Dry lithography using Alt-PSM could not give better CDU than immersion lithography using conventional illumination. Therefore, a strong RET was not required for immersion lithography to achieve the same CDU as dry lithography.
Sensitivity to coma and spherical aberration was evaluated. As mentioned above, conventional illumination with Att-PSM, annular illumination with Att-PSM and Alt PSM were optimized and used. The simulation conditions are shown in Table 2. Sensitivity was defined as CD changes per Zernike aberration (nm). Figure 2b shows the CD sensitivity against spherical aberration with a 100 nm defocus condition.

<table>
<thead>
<tr>
<th>Item</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aberrations</td>
<td>Z7, Z14 (coma), Z9, Z16 (spherical)</td>
</tr>
<tr>
<td>Patterns</td>
<td>80nm line and space, pitch=180nm</td>
</tr>
<tr>
<td></td>
<td>80nm line and space, pitch=240nm</td>
</tr>
<tr>
<td></td>
<td>80nm line and space, pitch=2000nm (Iso)</td>
</tr>
<tr>
<td></td>
<td>80nm line 2-bar, pitch=180nm</td>
</tr>
<tr>
<td>NA &amp; sigma setting and mask</td>
<td>Wet WC:0.93/0.80 Conv. + AttPSM</td>
</tr>
<tr>
<td></td>
<td>WA:0.93/0.75 2/3 Annular + AttPSM</td>
</tr>
<tr>
<td></td>
<td>WL:0.93/0.30 Conv. + AltPSM</td>
</tr>
<tr>
<td></td>
<td>Dry DC:0.90/0.80 Conv. + Att-PSM</td>
</tr>
<tr>
<td></td>
<td>DA:0.87/0.75 2/3 Annular + AttPSM</td>
</tr>
<tr>
<td></td>
<td>DL:0.93/0.30 Conv. + AltPSM</td>
</tr>
</tbody>
</table>

Figure 2b CD sensitivities of spherical aberration

Figure 2c Delta CD sensitivities in 2-bar of coma aberration
Dry lithography displayed 30-50% higher sensitivity to spherical aberration than immersion lithography. Immersion lithography was less sensitive to longitudinal aberrations because of its greater DOF. The sensitivity to spherical aberration of dry lithography with Alt-PSM was 1 nm/nm, the highest sensitivity among the conditions used in these evaluations. Coma aberration (lateral) generated a CD difference of 2-bar or placement error of the pattern. As shown in Figures 2c and 2d, it was clear that there was no great difference between dry lithography and immersion lithography. The CD difference of 2-bar for alt-PSM was large at 1 nm/nm for Z7 with dry exposure, and it was very small with conventional illumination.

Figure 2d Overlay sensitivities of coma aberration

Figure 2e CD sensitivities of sigma

Figure 2e shows the sensitivity of illumination sigma on CD. Conventional illumination with Att-PSM showed high sensitivity, which was different from aberration sensitivity. Immersion lithography displayed 20% lower sensitivity than dry lithography.

The sensitivity of aberration and illumination sigma for both immersion and dry lithography were studied. It was shown that immersion lithography had an advantage over dry lithography. In particular, immersion lithography can reduce the effect of a longitudinal aberration (such as spherical aberration) on CD by 30 - 50%.
The impact of the laser bandwidth E95 of the ArF excimer laser illumination source was also studied. The CD change of an 80 nm line pattern with 240 nm pitch and 2000 nm pitch was calculated with E95s of 0.3 - 0.7 pm under the given conditions of NA and sigma and shown in Table 2. Exposure was appropriate for an 80 nm line with 180 nm pitch printed onto 80 nm. Figure 2f shows an OPE curve under conventional illumination with Att-PSM. It was found that the effect of E95 on CD using immersion lithography is 20 - 30% smaller than with dry lithography (Figure 2g). The spectrum width of the light source caused chromatic aberration and reduced the image contrast through imperfect focus. Thus immersion lithography had an advantage because of its greater DOF.

### 3. SCANNER PERFORMANCE COMPARISON

In immersion lithography, filling the gap between the bottom lens of the projection optics and the wafer with water of refractive index 1.44 makes the incidence angle smaller and increases DOF by a factor of approximately 1.4, and can produce the effect of a NA greater than 1. In the partial-fill method, water is introduced only into the gap between the lens and wafer, to avoid leaving a water droplet behind on the wafer when the exposure is completed. Furthermore, there is a temperature control function in each part to compensate for temperature change due to water evaporation and prevent wafer deformation from causing overlay problems or focus instability to the extent possible.

In the past year, the overlay performance of immersion lithography has shown drastic improvement. Figure 3a shows the improvement of XT:1400Ei (ArF immersion) overlay performance. An 8 nm level was achieved in SMO under the present conditions, confirmed to be the same level of performance as with dry ArF for an XT:1400 (less than 8 nm).
Furthermore, 3 sigma of focus accuracy in a wafer is equal to or less than 40 nm, which is quite good (Figure 3b). This is also same level as dry scanner for an XT:1400 (equal to or less than 40 nm at 3 sigma).

Figure 3a Overlay improvement history of immersion scanner

Figure 3b Focus accuracy of immersion scanner

Figure 3c MA and MSD of immersion scanner
In immersion lithography the introduction of water and extraction of water and air can cause vibration at the edge of a wafer, leading to problems with scan synchronization. However this was found not to be a problem across the full wafer surface, as shown in Figure 3c for XT:1400Ei. The moving average (MA) of immersion lithography is equal to or less than 2 nm and moving standard deviation (MSD) is equal to or less than 8 nm. MSD is at a level that will produce no problems in imaging performance for a 55 nm logic device even though it is inferior to a dry scanner at levels equal to or less than 7 nm.

4. DEFECTIVITY

In the immersion resist process, a top coat is applied together with dry resist. The top coat is selected to match the resist, with an eye to controlling surface hydrophilicity. As shown in Figure 4, the defectivity, with a top coat resist process and an XT:1400Ei, is 10 and below, which is substantially similar to dry performance.

A possible concern is that the wafer stage surface will be contaminated by leaching of the photo resist and particles deposited by the water. To reduce the defect rate, it is important to establish periodic cleaning procedures for the lithography tool.

![Figure 4 Defectivity of immersion scanner](image)

![Figure 5 Patterning results of 55nm logic device by immersion scanner](image)
5. 55 NM LOGIC DEVICE EXPOSURE RESULTS

The result of immersion lithography for a 55 nm logic device, whose minimum pitch is 180 nm, is shown below. The imaging result for an XT:1400EI with an NA of 0.93 under conventional illumination is shown in Figure 5. It is clear that a DOF greater than 200 nm was achieved. In addition, the overlay performance of the gate-layer of the 55 nm logic device is shown in Figure 6a, and the Metal-1 layer in Figure 6b. Using a \(|\text{Mean}|+3 \sigma\) definition, \(X = 15.9\) nm, 12.6 nm, and \(Y = 22\) nm, 11.4 nm were achieved, confirming good performance.

![Figure 6a Overlay performance of 55nm logic device by immersion scanner, gate to STI](image)

![Figure 6b Overlay performance of 55nm logic device by immersion scanner, metal 1 to contact](image)

6. CONCLUSION

We have described for the advantages and disadvantages of NA < 1.0 immersion lithography.

Optical image simulation results show that CD uniformity can be improved by using immersion lithography. Strong RETs such as Alt-PSM is not required for immersion lithography to achieve the same CD uniformity as the dry lithography. From a view of sensitivity to lens aberration, immersion lithography reduces sensitivity to spherical aberration by 30-50% (one of the longitudinal aberrations). CD sensitivity to a variation in illumination sigma is 20% better with immersion lithography. Also, sensitivity to E95 laser bandwidth control is improved by 20-30%.

From a machine performance point of view, the overlay accuracy of immersion scanner has been significantly improved in the past year. Current overlay accuracy has reached the 8 nm level, which is almost equal to that of the dry-ArF tool. Focus control variation over the wafer also remains within 40 nm (3 sigma), which is also same level as the dry tool. For scan synchronization, the MA is less than 2 nm, the MSD is less than 8 nm. These key variables are almost identical to those of a dry-ArF exposure.
Furthermore, we detected fewer than 10 pattern defects which is same level as dry lithography using top coat resist process on XT:1400Ei.

Thus we can conclude that proof imaging and overlay performance results give every indication that the NEC Electronics 55 nm logic device “UX7LS” can be fabricated successfully with immersion lithography in volume mass production.

7. FUTURE ACTION/CHALLENGES

NEC Electronics will continue to pursue the cost savings offered by a top-coat-less resist process for immersion lithography. Additionally, improved in-situ cleaning methods will be required to achieve lower defect levels.

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REFERENCES